(12) **EUROPEAN PATENT APPLICATION**

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(54) Semiconductor devices having increased break-down voltage.

(57) In order to increase the breakdown voltage of a reverse-biased p-n junction (20) of a semiconductor device, at least three annular regions (1 to 6) which extend around the active device region (11) are located within the spread of a depletion layer (30) from the junction (20). At least one inner annular region (1,2,3) is wider than outer annular regions (4,5,6), and this increased width of the inner region or regions (1, etc.) reduces peak electrostatic fields found to occur at the bottom outer corners (20', 21' etc.) of the active device region (11) and inner annular regions (1, etc.). The spacing of the annular regions (1 to 6) increases with remoteness from the active device region (11), although at least two inner annular regions (1,2) may have the same spacing as that of the innermost annular region (1) from the active device region (11). A group of annular regions (2,3 and or 4,5,6) may have the same width as each other in the group.
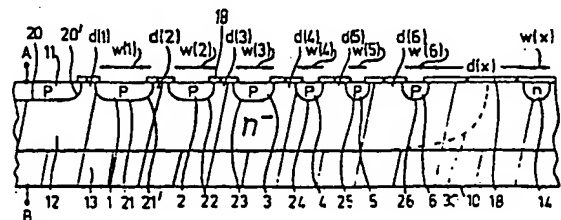
Fig. 1.

SEMICONDUCTOR DEVICES

The invention relates to semiconductor devices, for example rectifier diodes, field-effect transistors, bipolar transistors and thyristors, having a p-n junction which is operated under reverse bias in at least one
5 mode of operation of the device.

The article entitled "High Voltage Planar P-N Junctions" by Y.C. Kao and E.D. Wolley in the "Proceedings of the I.E.E.E.", Vol. 55, No. 8, August 1967, pages 1409 to 1414 describes semiconductor devices having a concentric field-limiting planar junction structure to increase the
10 breakdown voltage. These devices comprise a semiconductor body having a portion of one conductivity type adjoining a major surface of the body. An active device region of the opposite conductivity type also adjoins said major surface and forms with said portion a main p-n junction which terminates at said major surface and which is operated under reverse bias
15 in at least one mode of operation of the device. At least three annular regions of said opposite conductivity type extend around said active device region. These annular regions also adjoin said major surface and form with said portion auxiliary p-n junctions located within the spread of a depletion layer from the reverse-biased main p-n junction so as to
20 increase the breakdown voltage of the main p-n junction. The spacing between two outer annular regions which are remote from the active device region is larger than the spacing between the active device region and an inner annular region which is adjacent the active device region. Said active device region and said annular regions are more highly doped than
25 said portion of the body.

It is stated in the Proc. I.E.E.E. article that in the absence of the annular regions, a significantly higher electric field occurs at the surface-terminating portion of the (main) p-n junction than at the bulk portion which extends parallel to the surface, so resulting in avalanche
30 breakdown of the p-n junction at the surface. The provision of the annular regions reduces the field at the surface so that breakdown does not occur until a higher voltage level which is comparable with the plane breakdown voltage of the bulk portion of the junction. The annular regions are spaced such that, at a voltage considerably less than the
35 breakdown voltage of the bulk portion of the main junction, the space charge region of the main junction punches through to the first annular region. After the punch-through, further increases in voltage are largely

taken up by the first annular region as the carriers are depleted on the outside of the annular region junction. The maximum electric field occurring across the main junction adjacent the surface is determined by the punch-through voltage and so can be controlled to be considerably less than the critical field, by adjusting the spacings. Thus the annular regions act like voltage dividers with the voltage between the main junction and the annular regions being a function of the spacing.

As illustrated in Figure 3 of said Proc. I.E.E.E. article, in the devices fabricated and studied by Kao and Wolley the spacing between adjacent annular regions is larger remote from the active device region than adjacent the active device region. As stated in said article, this variable spacing was selected in order to study variation of punch-through voltage on a single structure. However it has subsequently been found that by varying the spacing in this manner a higher breakdown voltage can be achieved compared with a concentric annular structure of uniform spacing. All the annular regions of each individual device are of uniform width; Kao and Wooley state in the related U.K. Patent Specification (GB) 1,138,237A that their width is not important and can be made as narrow as feasible in order to retain as much area on the semiconductor body as possible for the main p-n junction. All the annular regions of each individual device described in GB 1,138,237A are also of uniform width.

The present invention is based on a surprising discovery by the present inventor that the width of the annular regions (as well as their spacing) is important for optimising the voltage performance.

Thus, according to the present invention, there is provided a semiconductor device comprising a semiconductor body having a portion of one conductivity type adjoining a major surface of the body, an active device region of the opposite conductivity type also adjoining said major surface and forming with said portion a main p-n junction which terminates at said major surface and is operated under reverse bias in at least one mode of operation of the device, and at least three annular regions of said opposite conductivity type extending around said active device region, which annular regions also adjoin said major surface and form with said portion auxiliary p-n junctions located within the spread of a depletion layer from the reverse-biased main p-n junction so as to increase the breakdown voltage of the main p-n junction, the spacing between two outer annular regions which are remote from the active device

region being larger than the spacing between the active device region and the inner annular region which is adjacent the active device region, said active device region and said annular regions being more highly doped than said portion of the body, characterised in that the inner annular region

5 which is adjacent the active device region is wider than said two outer annular regions which are remote from the active device region.

Surprisingly it has been found that by having at least one wider inner annular region adjacent the active device region a higher percentage of the plane breakdown voltage can be achieved while the total surface

10 area of the body occupied by the concentric annular region structure can be reduced by having narrower annular regions remote from the active device region. The Applicants believe that the increase in breakdown voltage is related to a reduction in curvature of the equipotential surfaces in the depletion layer adjacent the outer bottom corner of the

15 active device region and the inner annular region(s) so reducing the electrostatic field due to the field lines being stretched apart by the larger width of the inner annular region(s). The effect is particularly important for shallow regions, for example when the main and auxiliary junctions extend to a depth of about 5 microns or less from the major

20 surface of the body. For a given spacing between the regions, shallow regions introduce more curvature into the equipotential surfaces thus increasing the field strengths and reducing the breakdown voltage.

The number, widths and spacings of the annular regions depend on the desired breakdown voltage. Three annular regions may be sufficient for

25 some low voltage devices, the inner annular region being wider than the two outer annular regions. Usually more than three annular regions will be provided, especially for devices with shallow junctions. Thus, as junction depth is reduced, a larger number of annular regions are normally required to support a given voltage. For example a device having a

30 breakdown voltage in excess of 500 volts and having a depth of about 3 micrometres for the main and auxiliary $\underline{p-n}$ junctions may have a series of at least 4 or more concentric annular regions. Especially for shallow junctions, in order to reduce curvature of the equipotential surfaces while obtaining a compact structure, the width of the inner(most) annular

35 region may be at least six or more times the spacing of the innermost annular region from the active device region, more than seven times its depth, and at least two or more times the width of an outer annular

region. For higher voltage devices many more outer annular regions may be added and the width of the innermost annular region may be considerably increased. For example, a device having a breakdown voltage of at least 1,000 volts and a junction depth of about 3 micrometres, may have a series 5 of between ten and fifteen annular regions, the innermost of which may have a width of more than fifteen times its spacing from the active device region, more than twelve times its depth, and more than six times the width of the outermost annular region.

The annular regions may comprise at least one group of at least two 10 successive annular regions which have the same width as each other in the group. This simplifies design analysis of the annular regions and is particularly acceptable for a group of annular regions which are not immediately adjacent the active device region. Thus, between the active device region and the group of annular regions of the same width, there 15 may be at least one innermost annular region which is wider than the regions of said group. The width of the one or more wider innermost regions can be individually chosen to optimise the stretching apart of the electrostatic field lines. However, for some devices it may be sufficient for the wider innermost annular regions to constitute a group having the 20 same region width as each other but wider than the region width of the other group.

In order to control and optimise the breakdown voltage it is generally desirable to vary the spacing of the annular regions so that the spacing is larger remote from the active device region. Thus, the spacing 25 between said two outer annular regions remote from the active device region is larger than the spacing between the active device region and the innermost annular region. However, preferably the innermost annular region is so wide that the spacing between said two outer annular regions is smaller (for example, a half or less) than the width of the innermost 30 annular region. The spacing between outer annular regions which are remote from the active device region preferably increases progressively in accordance with remoteness from the active device region to optimise the spread of the depletion layer to these narrower remote annular regions. The inventor has found that,

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contrary to simple theory, relatively small changes in the spacing of these remote annular regions can even have a significant effect on the electrostatic field and avalanche breakdown at the junctions of the active device region and the inner annular regions. This is particularly useful where the close spacing of the inner annular regions from each other and from the active device region may be limited by technological constraints on reliably reproducible smallest separation distances, for example as determined by lateral etching of juxtaposed mask windows and lateral diffusion of juxtaposed regions in technological processes commonly used to form such devices. Thus the same close spacing may be used for at least two annular regions near the active device region as well as the spacing between the active device region and the innermost annular region.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a diagrammatic cross-section through part of a semiconductor device in accordance with the present invention;

Figure 2 is a graph of the hole avalanche integral I_p against the number N of each of the annular regions (1 to 6) of one particular example of the device of Figure 1, and

Figure 3 is a graph similar to that of Figure 2, but in respect of a modified example of the device of Figure 1.

The semiconductor device of Figure 1 comprises a semiconductor body 10 (for example of monocrystalline silicon) having a portion 12 of one conductivity type (n-type, in the example shown in the drawing) which adjoins the upper major surface of the body 10. An active device region 11 of the opposite conductivity type (p-type, in the example shown) also adjoins said upper major surface and forms with the body portion 12 a main p-n junction 20 which terminates at the upper major surface. The junction 20 is operated in reverse-bias in at least one mode of operation of the device, by applying a bias voltage between the electrodes A and B in Figure 1.

Concentric annular regions 1 to 6 of said opposite conductivity type (p-type, in the example) extend around the active device region 11. These annular regions 1 to 6 also adjoin the upper major surface and form with the body portion 12 auxiliary p-n junctions 21 to 26 within the

spread of a depletion layer 30 from the reverse-biased main p-n junction
20 so as to increase the breakdown voltage of the main junction 20.
In Figure 1 an example of a depletion layer 30 is shown as extending
across the thickness of the body portion 12, although in some cases the
5 depletion layer 30 may not extend so deeply from the junction 20.

The active device region 11 and annular regions 1 to 6 are more
highly doped than the body portion 12 and may be formed by locally
implanting or/and diffusing dopant of the opposite conductivity type
(p-type) to locally overdope the body portion 12. Figure 1 illustrates
10 an insulating passivating layer 18 (for example of silicon dioxide) on
the upper major surface of the body 10 and having openings serving
as mask windows through which this local dopant introduction may be
effected to form the regions 1 to 6 and 11. Depending on the type of
device, a further insulating passivating layer may be provided in these
15 openings to passivate exposed areas of the upper major surface of the
body 10 except where contacted by electrodes. A highly doped
channel-stopper region 14 of the same conductivity type as the body
portion 12 extends in a concentric arrangement around the system
of regions 1 to 6 and is formed by local dopant introduction in a
20 separate step from the regions 11 and 1 to 6.

The annular regions 1 to 6 and 14 may be circular rings which have
circular symmetry around the active device region 11 at the upper
major surface of the body 10. However, other geometrical outlines
are possible, depending on the outline of the active device region 11
25 and the type of the device. Thus, for example the region 11 may have a
square outline with straight sides but with rounded corners, and the
concentric rings 1 to 6 and 14 may be similarly square with straight
sides and rounded corners. Such different outlines and geometries are
already known in the power semiconductor device art and so will not be
30 described further in the present specification. For convenience and
simplicity in the drawing, Figure 1 merely shows a cross-section through
part of the region structure 11, 1, 2, 3, 4, 5, 6 and 14 at the right-hand
side of the active device region 11.

The basic device structure of Figure 1 may be used for various
35 types of semiconductor device in accordance with the invention, for

example a power rectifier diode, a high voltage bipolar transistor,
a thyristor, or a high voltage insulated-gate field-effect transistor.
For a power rectifier diode, the p-n junction 20 may constitute
the rectifying junction, metal layers forming the electrodes A and B

5   constitute the diode terminals, and the body portion 12 may be a high
resistivity n-type substrate into which a highly-doped n-type layer 13
is diffused at the lower major surface and into which the p-type
regions 11, 1 to 6 are diffused at the upper major surface. In the
case of an insulated-gate field-effect transistor, the p-n junction 20

10 may constitute the drain junction formed by an annular p-type drain
region 11 which extends around a central p-type source region and an
intermediate channel region of the transistor, and the body portion 12
may be a high resistivity n-type epitaxial layer on a highly-doped
n-type substrate 13 to which the p-type source region may be short-

15 circuited in known manner.

          In the case of a bipolar transistor, the p-n junction 20
constitutes a base-collector junction of the transistor, the region 11
being the p-type base region which is provided in a high resistivity
n-type epitaxial layer 12 on a highly-doped n-type substrate 13. The

20 electrodes A and B are base and collector terminals respectively of the
transistor, and at least one highly-doped n-type emitter region having its
own electrode is provided in the base region 11. However the main
p-n junction 20 may even be one blocking junction of a thyristor structure.
In this latter case, the Figure 1 structure is modified to have for

25 example a high resistivity n-type substrate 12 into which p-type regions
11 and 13 may be diffused to form two oppositely-located blocking
p-n junctions, the p-type region 13 constituting the anode of the
thyristor while an n-type cathode emitter is provided in the p-type
base region 11.

30   The series of concentric annular regions 1 to 6 serves to increase
the breakdown voltage of the p-n junction 20 by widening the spread of
the depletion layer 30 along the body surface so as to reduce the
associated electrostatic field adjacent the surface to a value less
than that of the critical field for electron-hole pair generation by

35 avalanche breakdown. The inventor has found that a peak electrostatic
field occurs in the depletion layer 30 adjacent the outer bottom

corner 20' of the active device region 11 and/or adjacent the outer
bottom corner 21' etc. of the inner annular region(s) 1 etc. This peak
electrostatic field results from curvature of the equipotential surfaces
adjacent these corners, especially when the regions 11, 1, etc. and

5   the junctions 20, 21, etc. are of shallow depth, e.g. less than
10 micrometres. If the annular regions 1 to 6 are of known configuration
the breakdown voltage of the main junction 20 may then be limited by
avalanche breakdown from one of these peaks.

In accordance with the present invention this peak electrostatic

10   field is reduced so increasing the breakdown voltage by having one or
more wider annular regions (e.g. regions 1, 2 and 3 in Figure 1) adjacent
the active device region 11. The reduction in the peak field adjacent the
corners 20', 2.', etc. is thought to result from the field-lines being
stretched apart by the increased width of the inner annular regions

15   (e.g. regions 1, 2 and 3 in Figure 1). The annular regions (e.g.
regions 4, 5 and 6) which are remote from the active device region 11
are of narrower width, as illustrated in Figure 1. This is useful in
reducing the surface area required to accommodate the total annular
region system especially where the spacing of the annular regions 1 to 6

20   increases with remoteness from the active device region 11, and the
inventor has found that, contrary to simple theory, relatively small
changes in the spacing of these narrower outer annular regions (e.g.
regions 4, 5 and 5 of Figure 1) can have a significant effect in reducing
the electrostatic field at the junctions 20, 21, 22 etc. of the active

25   device region 11 and wider inner annular regions (e.g. regions 1, 2 and 3).

It should be noted that Figure 1 is not drawn to scale and that the
proportions and especially the thickness/depth of various portions of the
drawing have been exaggerated or reduced for the sake of clarity and
convenience in the drawing. The precise number, widths and spacings of

30   the annular regions depend on the desired breakdown voltage and the depths
of the regions, and these are chosen as appropriate to the type of device.
By way of illustration for Figure 1, Table 1 gives an example of suitable
widths (w) and spacings (d) in micrometres for a concentric arrangement
of six $\underline{p}$-type annular regions 1 to 6 for a device having an operating

35   voltage of about 500 volts across the main $\underline{p}$-$\underline{n}$

junction 20. the regions 11 and 1 to 6 being diffused to a depth of 3.25 micrometres and having a surface doping concentration of 7×10^{18} cm^{-3}, the body portion 12 having a doping concentration of 2.5×10^{14} cm^{-3} and a thickness of 44 micrometres.

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TABLE 1

Spacing/Width	Micrometres
d(1)	2 ; 7
w(1)	25 ; 20
d(2)	2 ; 7
w(2)	15 ; 10
d(3)	3 ; 8
w(3)	15 ; 10
d(4)	4 ; 9
w(4)	10 ; 5
d(5)	5 ; 10
w(5)	10 ; 5
d(6)	7 ; 12
w(6)	10 ; 5
d(x)	25 ; 30
w(x)	10 ; 5

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In the second column of Table 1 the first value is the actual spacing or width of the regions in the final device assuming a 30 lateral diffusion of about 2.5 micrometres for the regions 1 to 6, 11 and 14 in the body portion 12, whereas the second value relates to the dimensions of the mask 18 and its windows through which the regions 1 to 6, 11 and 14 were diffused.

In the example of Table 1, the width w(1) of the innermost 35 annular region 1 is more than seven times its depth, more than twelve

times the spacing d(1) of the region 1 from the active device region 11 and more than twice the width w(6) of the outermost annular region 6. The regions 4, 5 and 6 form an outer group of annular regions having the same width as each other, and the regions 2 and 3 form an inner group having the same larger width as each other. The innermost region 1 is even wider than the regions 2 and 3. The spacing d(4), d(5), d(6) between annular regions 4, 5 and 6 remote from the active device region 11 is larger than the spacing d(1) between the active device region 11 and the innermost region 1 but less than a third of the width w(1) of the wide innermost region 1. The spacing d(4), d(5), d(6) between annular regions 3, 4, 5 and 6 which are remote from the active device region 11 increases progressively in accordance with the remoteness from the active device region 11. The regions 1 and 2 have the same spacing d(2) from each other as the spacing d(1) between the active device region 11 and the innermost annular region 1, and this spacing d(1), d(2) corresponds to the minimum reliably reproducible separation distance between the diffused regions 11, 1 and 2.

Figure 2 provides an illustration of avalanche breakdown performance obtained by subjecting the example of Table 1 to a numerical analysis of the electrostatic field and floating potentials associated with each annular region 1 to 6 as a function of the reverse-bias potential of the main junction 20. The numerical analysis was carried out with the aid of a computer employing a finite difference algorithm using routines such as those described by H. L. Stone in the Journal of the Society for Industrial and Applied Mathematics (SIAM) on Numerical Analysis, Vol. 5, (1968), pages 530 to 552. Depletion region logic such as described by U. A. K. Temple and M. S. Adler in I.E.E.E. Transactions on Electron Devices, Vol. ED-22, No. 10, (1975), pages 910 to 916, was used to avoid time-consuming complications of evaluating exponential functions to obtain carrier concentrations which are not generally significant to off-state analysis. The floating potential regions were treated in a similar manner to that described by M. S. Adler, U. A. K. Temple, A. P. Ferro and R. C. Rustay in I.E.E.E. Transactions on Electron Devices, Vol. ED-24, No. 2, (1977), pages 107 to 113, i.e. the entire junction boundary of each region is searched individually after each iteration to determine the point of minimum reverse bias

or maximum forward bias of that region and the potential of that region
is then adjusted so that carrier injection through that point of
minimum reverse bias or maximum forward bias is only just prevented.
Having established in this manner a computer model of the potential
5   distribution of the total concentric region arrangement for a given
reverse bias of the main junction 20, the electrostatic field lines
passing through the field peak of each region were determined,
and avalanche integrals (such as described by R. van Overstraeten and
H. de Man in Solid State Electronics, Vol. 13, (1970), pages 583 to 608)
10 were evaluated along these field lines. The actual algorithm used
is not important to the understanding of the present invention and so
no further details are given in the present specification.

Avalanche integrals less than or at most equal to unity are required
for a safe design avoiding avalanche breakdown at the maximum reverse
15 bias voltage. When analysing breakdown performance of the annular region
system only the hole avalanche integral Ip computed from the field peak
within each annular region need be considered, as this is a much stronger
function of electrostatic field than the electron avalanche integral In.
Furthermore if In equals 1.0, then Ip also equals 1.0; if In is less than
20 1.0, then Ip is also less than 1.0; or if In is greater than 1.0, then
Ip is also greater than 1.0.

Figure 2 shows a plot of the avalanche integral Ip (computed in
this manner for the example described above) as a function of the
different p-type regions having reference numbers 11,1,2,3,4,5 and 6
25 in Figures 1 and 2. The widths (w) and spacings (d) of the various
regions which have a depth of 3.25 micrometres are given in Table 1.
The reverse-bias voltage across the p-n junction 11 was 550 volts.
It can be seen from Figure 2 that the highest hole avalanche integral
in this region system is associated with the active device region 11
30 and main junction 20, but this highest hole avalanche integral
(about 0.9) is less than the critical 1.0 value for avalanche breakdown.

Figure 3 is a similar plot with 550 volt reverse-bias, but for a
modified example of Figure 1. This modified example has the same
region depth and the same values of d(1) to d(6), d(x), w(2) to w(6),
35 and w(x) as in Table 1, but the width w(1) of the innermost annular

region 1 is reduced to 15 micrometres (10 micrometres width for the mask window) instead of the previous 25 micrometres. The inner regions 1, 2 and 3 in this modified example therefore form one group of wide annular regions having the same width as each other. As can be seen

5 by comparing Figures 2 and 3, this reduced width of the wide innermost annular region 1 increases the hole avalanche integral Ip for the active device region 11 and main junction 20 where this avalanche integral is now slightly greater than the critical 1.0 value. Analysis of the computer model suggests that this increase in avalanche integral

10 is associated with a slight increase in curvature of the equipotential lines adjacent the outer bottom corner 20' of the junction 20. The device structure of Figure 3 has a breakdown voltage lower than 550 volts, but the avalanche integral increase is maintained sufficiently small by the larger width of regions 1, 2 and 3 compared

15 with regions 4, 5 and 6 that the device may still be operated at voltages up to about 500 volts. However, the structure of Figure 3 is less advantageous than that of Figure 2 (Table 1) because with the increased avalanche integral it may be more susceptible to premature breakdown due to effects which charge-states in the insulating layer 18

20 may have on the electrostatic field in the underlying depletion layer or to the effects of manufacturing tolerances in defining the regions. It will therefore be preferable to operate the device having the annular region system of Figure 3 at a slightly lower voltage than that of Figure 2.

25   In an annular region system not in accordance with the present invention and having all the regions 1 to 6 of the same width (10 micrometres) as each other and with the same depth (3.25 micrometres), the hole avalanche integral Ip adjacent the main junction 20 increases to greater than unity with even lower applied reverse bias voltages.

30 Thus, in this case avalanche breakdown occurs at a lower voltage in spite of maintaining an increased spacing of the annular regions with distance from the active device region 11. The numerical analysis indicates that the increase in avalanche integral Ip in this case results from a peak field associated with curvature of the equipotential lines

35 adjacent the bottom outer corners 20', 21', etc. of the inner junctions 20, 21 etc.

It will be evident that many modifications are possible within
the scope of this invention. Thus, for example in the case of a
power rectifier diode the rectifying junction of the diode may be
formed by a metal-semiconductor Schottky contact to the body
5   portion 12 and this junction may be bounded at its edge by an
annular guard region 11 which constitutes the active device region
of said opposite conductivity type.

Higher voltage devices may be manufactured using a higher
resistivity body portion 12 and by adding even wider inner annular
10   regions adjacent the active device region. Thus, a device having a
breakdown voltage of at least 1,000 volts may have a body portion
with a doping concentration of 10^{14} cm^{-3} and a thickness of at
least 90 micrometres, and there may be between ten and fifteen
annular regions 1,2 etc. having spacings and widths in accordance
15   with the invention, of which at least one innermost annular region
may be as much as fifteen or more times as wide as the spacing d(1)
from the active device region 11 and as much as six or more times
as wide as outermost annular regions. The precise number, widths
and spacing of these annular regions 1,2 etc. in accordance with
20   the invention can be optimised for 1,000 volt operation even with
such shallow depths of 3 or 5 micrometres for the active device
region 11 and annular regions 1,2 etc. In some devices, in
addition to providing wider inner annular regions between the
active device region and narrow outer annular regions, it may be
25   acceptable or even desirable to provide a wide annular region
between two of these narrow outer annular regions in order to
reduce the field at that location.

It will also be evident that the conductivity types of all the
regions of the device may be reversed to form opposite conductivity
30   type devices. Furthermore semiconductor materials other than
silicon may be used for the devices, although allowance must then
be made for different critical field strengths for avalanche
breakdown in such other semiconductor materials. Instead of an
insulating layer on the body surface, the regions 11, 1 to 6, and
35   14 may be passivated with a semi-insulating layer or a combination
of insulating and semi-insulating layers.

CLAIMS:

1.   A semiconductor device comprising a semiconductor body having a portion of one conductivity type adjoining a major surface of the body, an active device region of the opposite conductivity type also adjoining said major surface and forming with said portion a main p-n junction which terminates at said major surface and is operated under reverse bias in at least one mode of operation of the device, and at least three annular regions of said opposite conductivity type extending around said active device region, which annular regions also adjoin said major surface and form with said portion auxiliary p-n junctions located within the spread of a depletion layer from the reverse-biased main p-n junction so as to increase the breakdown voltage of the main p-n junction, the spacing between two outer annular regions which are remote from the active device region being larger than the spacing between the active device region and the inner annular region which is adjacent the active device region, said active device region and said annular regions being more highly doped than said portion of the body, characterised in that the inner annular region which is adjacent the active device region is wider than said two outer annular regions which are remote from the active device region.

2.   A semiconductor device as claimed in Claim 1, further characterised in that the width of said inner annular region is as least twice the width of at least one of the outer annular regions.

3.   A semiconductor device as claimed in Claim 1 or Claim 2, further characterised in that the width of said inner annular region is at least six times the spacing of said inner annular region from the active device region.

4.   A semiconductor device as claimed in anyone of the preceding Claims, further characterised in that the width of said inner annular region is more than seven times the depth of said inner annular region.

5.   A semiconductor device as claimed in anyone of the preceding Claims, further characterised in that the annular regions comprise at least one group of at least two successive annular

regions which have the same width as each other in the group.

6. A semiconductor device as claimed in Claim 5, further characterised in that between the active device region and the group of annular regions of the same width there is at least one innermost annular region which is wider than the regions of said group.

7. A semiconductor device as claimed in anyone of the preceding Claims, further characterised in that the width of the inner annular region is larger than the spacing between said two outer annular regions remote from the active device region.

8. A semiconductor device as claimed in Claim 7, further characterised in that there are at least two inner annular regions near the active device region which have the same spacing from each other as the spacing between the active device region and the innermost annular region.

9. A semiconductor device as claimed in anyone of the preceding Claims, further characterised in that the spacing between outer annular regions which are remote from the active device region increases progressively in accordance with remoteness from the active device region.

Fig.1.

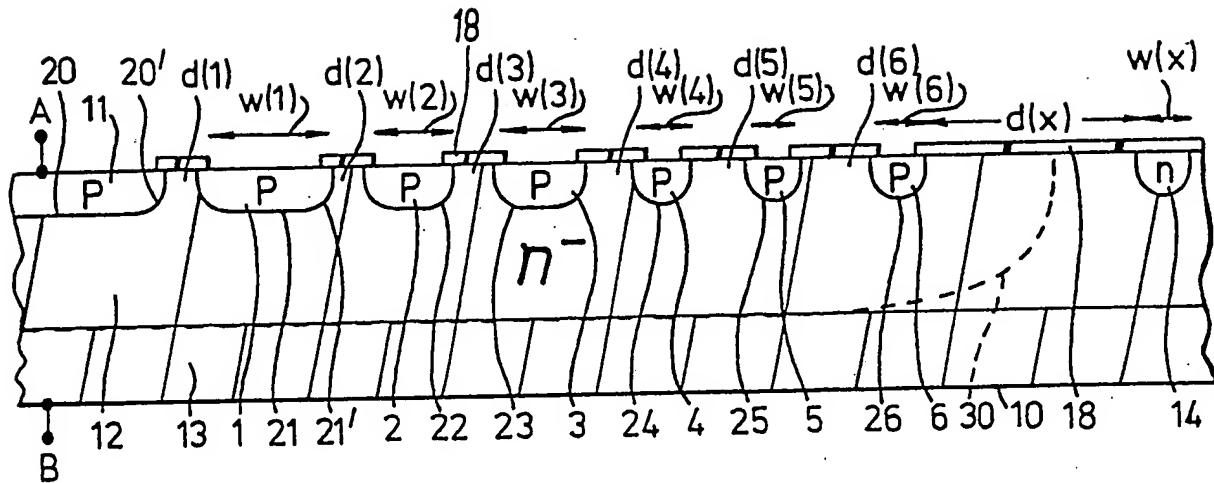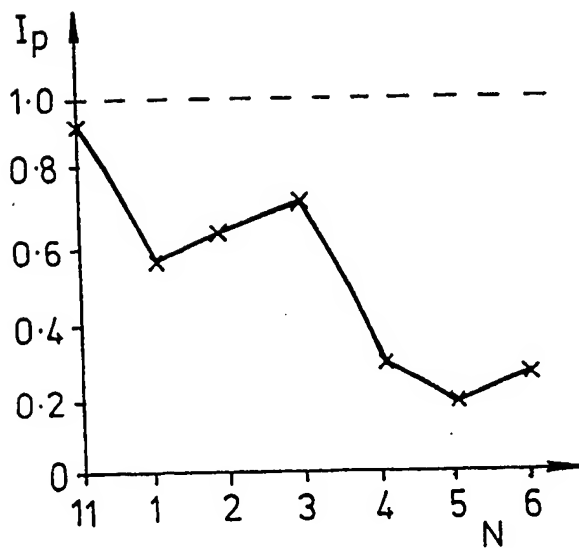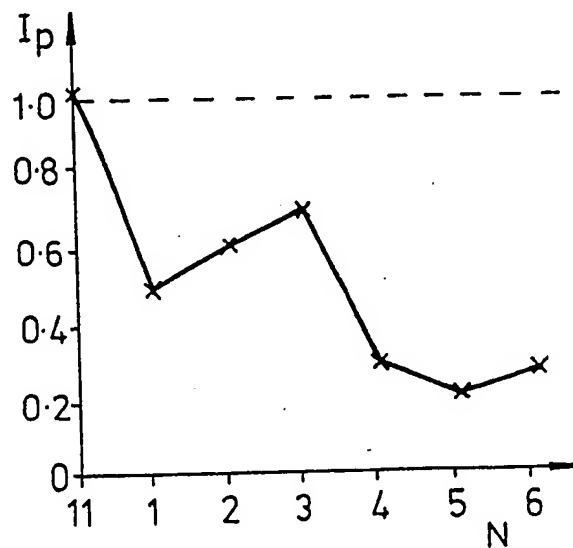

Fig.2.

Fig.3.